

AMENDMENT AND RESPONSE

Serial Number: 08/903,486

Filing Date: July 29, 1997

Title: SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS

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IN THE CLAIMS

1.(Amended) A transistor comprising:

sub D1
A1
a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion, and an electrically interconnected gate formed of a silicon carbide material.

6.(Amended) The transistor of claim 1, wherein the silicon carbide gate material is described by $\text{Si}_{1-X}\text{C}_X$ and X is approximately less than or equal to 0.5.

15.(Amended) A semiconductor memory device comprising:

sub D3
A2
a memory array including a plurality of transistors, at least one of the transistors in a semiconductor surface layer formed on an underlying insulating portion and including an electrically interconnected gate formed of a silicon carbide material;
addressing circuitry for addressing the memory array; and
control circuitry for controlling read, write, and erase operations of the memory device.

Please add the following new claims:

sub E1
22.(New) The integrated circuit device of claim 11 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

sub D4
23.(New) The semiconductor memory device of claim 11 wherein each silicon carbide gate comprises $\text{Si}_{1-X}\text{C}_X$ and X is approximately less than or equal to 0.5.

24.(New) The semiconductor memory device of claim 15 wherein each of the transistors in the memory array comprises:

sub D4
a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion; and

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an electrically interconnected gate formed of a silicon carbide material.

Sub (C2)
25.(New) The semiconductor memory device of claim 15 wherein pairs of the transistors in the memory array comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer; and

A3
an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer.

Sub E1
26.(New) The semiconductor memory device of claim 25 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

Sub (C3)
27.(New) The semiconductor memory device of claim 15 wherein the silicon carbide gate comprises polycrystalline silicon carbide.

28.(New) The semiconductor memory device of claim 15 wherein the silicon carbide gate comprises microcrystalline silicon carbide.

29.(New) The semiconductor memory device of claim 15 wherein the silicon carbide gate is separated from the semiconductor surface layer by an insulating layer of silicon oxide.

30.(New) The semiconductor memory device of claim 15 wherein the silicon carbide gate comprises $\text{Si}_{1-X}\text{C}_X$ and X is approximately less than or equal to 0.5.

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31.(New) A semiconductor memory device comprising:
a memory array including a plurality of transistors wherein pairs of the transistors
comprise:
a substrate;
a p-channel transistor formed in a first portion of the substrate, the p-channel
transistor including a source region, a drain region, a channel region between the source and
drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and
separated therefrom by an insulating layer; and
an n-channel transistor formed in a second portion of the substrate, the n-channel
transistor including a source region, a drain region, a channel region between the source and
drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and
separated therefrom by an insulating layer;
addressing circuitry for addressing the memory array; and
control circuitry for controlling read, write, and erase operations of the memory device.

32.(New) The semiconductor memory device of claim 31 wherein the substrate comprises a
semiconductor surface layer formed on an underlying insulating portion.

33.(New) The semiconductor memory device of claim 31 wherein each silicon carbide gate
comprises polycrystalline silicon carbide.

34.(New) The semiconductor memory device of claim 31 wherein each silicon carbide gate
comprises microcrystalline silicon carbide.

35.(New) The semiconductor memory device of claim 31 wherein each an insulating layer
comprises silicon oxide

36.(New) The semiconductor memory device of claim 31 wherein each silicon carbide gate
comprises $\text{Si}_{1-X}\text{C}_X$ and X is approximately less than or equal to 0.5.